ABSTRACT OF THE DISCLOSURE

A bus data signal is applied to a tapped data delay line of selected step size and whose overall delay is at least one (maximum) unit interval. The various increasingly delayed data values present at the taps of the delay line are clocked into respective cells of a sticky ZEROs register previously initialized to all ONEs, and into respective cells of a sticky ONEs register previously initialized to all ZEROs. The sticky ZEROs register SZERO measures UI(ONE), which is the unit interval of a ONE. Assuming that the active edge of a bus signal is the rising edge, the inversion of the selected data signal is used to clock SZERO, while the non-inverted signal clocks SONE. Over a period of time following initialization, the data signal can be expected to experience isolated ONEs (i.e., a single ONE with ZEROs before and after) and similarly isolated ZEROs. A ONE to ZERO transition in the data will clock any far-to-the-right ZEROs in the delay line into SZERO, which become sticky and trim the indication of UI(ONE) in left-most and remaining initial ONEs. In similar fashion, a ZERO to ONE transition in the data will clock any far-to-the-right ONEs in the delay line into SONE, which become sticky and trim the indication of UI(ZERO) in left-most and remaining initial ZEROs.